Roll No										

B.E./B.Tech.(Full Time) DEGREE END SEMESTER EXAMINATION, APR/MAY 2012.

INFORMATION TECHNOLOGY BRANCH

THIRD SEMESTER

IT 9201 – COMPUTER ORGANIZATION

(REGULATIONS 2008)

Time: Three Hours Max.Marks: 100

Answer All Questions

PART-A (10 X 2 = 20 Marks)

1. Express the following number in decimal : $(10010.0101)_2$
2. Express the Boolean function F=B'+A'C as a sum of minterms. The function has three variables: A,B, and C.
3. Design a 4-bit Adder-Subtractor.
4. What is the difference between serial and parallel transfer? What type of register is needed to convert serial data to parallel and parallel to serial?
5. Compare RISC vs CISC.
6. List the parameters that affect the processor performance.
7. Distinguish between Hardwired control and Micro-programmed control.
8. What is structural hazard? Give example.
9. List the sequence of events involved in handling an interrupt request from a device.
10. What is Hit rate and Miss Penalty?

PART-B (5 x 16 = 80 Marks)

11. a. i) Simplify the following Boolean expression to A) Sum-of-product
B) Product-of-sum using K-map (8)

B'D + A'BC' + AB'C + ABC'

ii) Simplify the following Boolean function using Tabulation method (8)

$F(w, x, y, z) = \sum (0, 2, 3, 5, 7, 9, 10, 11, 14, 15)$

12. a. i) With neat diagram explain the BCD Adder. (8)

ii) Write short note on Magnitude comparator and Decoder. (8)

(OR)

b. i) A sequential circuit has 2 D flip-flops A and B, two inputs x and y, one output z is specified by the following next-state and output equations (10)

$A(t+1) = x'y + xB$

$B(t+1) = x'A + xB$

$z = A$

A) Draw the logic diagram of the circuit. (4)

B) List the state table for the sequential circuit. (3)

C) Draw the corresponding state diagram (3)

ii) With neat diagram explain the 4-bit universal shift register. (6)

13. a. i) Explain in detail the various addressing modes with example. (8)

ii) Write and Explain the Restoring Division algorithm with example. (8)

(OR)

b. i) Explain the concept behind Booth's multiplication algorithm. What are its advantages? Multiply the following signed 2's complement numbers using the Booth's multiplication technique. A=011011 & B=101110 (8)

ii) With neat diagram explain the Floating-point addition-subtraction unit. (8)

14. a. i) What is Data hazard? Explain the methods to handle Data hazard with example. (8)

ii) Give the Single-bus organization of the datapath inside a processor. Write the sequence of control steps required for executing the following instruction:

ADD (NUM), R1 -> Add the contents of memory location NUM to register R1. (8)

(OR)

b. i) Explain in detail the Hard-wired control unit. (8)

ii) What is Instruction hazard? Explain the various methods to handle unconditional branch hazards. (8)

15. a. i) A byte addressable computer has a small data cache capable of holding eight 32-bit words. Each cache block consists of one 32-bit word. When a given program is executed the processor reads data from the following sequence of hex addresses:

200,204,208,20C,2F4,2F0,200,204,218,21D,24D,2F4,2F8

A) Show the contents of the cache at the end of each pass through this loop if a direct mapped cache is used. (5)

B) Repeat part (A) for an associative-mapped cache that uses the LRU replacement algorithm. (6)

C) Repeat part (A) for four-way set-associative cache. (5)

(OR)

b. i) With neat diagram explain the virtual memory organization and its address translation. (8)

ii) Write short notes on DMA Controller. (8)