Reg. No

B.E./B.Tech.(Full Time) DEGREE END SEMESTER EXAMINATIONS,APRIL/MAY 2012
COMPUTER SCIENCE & ENGINEERING BRANCH
SECOND SEMESTER
CS9152 – DIGITAL PRINCIPLES AND SYSTEM DESIGN
(REGULATION 2008)

Time: Three Hours **Max.Marks: 100**

PART A (10 x 2 = 20 Marks)
Answer All Questions.

1. Given two binary numbers X = 1010100 and Y = 1000011, perform the subtraction Y-X using 2's complement.
2. Simply the following Boolean expressions using four variable maps.
   wxy+yz+xy′z+x′y
3. Design a 4 bit combinational circuit incrementer using half adder.
4. Draw the graphic symbol of three state buffer gate and how is it different from normal buffer?
5. Give the differences between flip-flops and latches.
6. Construct a J K flip-flop using a D flip-flop, a 2-to-1 line multiplexer and an inverter.
7. Give the purpose of memory decoding.
8. List the eight unused states in the switch-tail ring counter and determine the next state for each of these states.
9. Discuss the fundamental mode of an asynchronous sequential circuit.
10. Give the purpose of race free state assignment.

PART – B (5 x 16 = 80 Marks)

11 (i) Design a counter with the following repeated binary sequence : 0, 1, 2, 3, 4, 5, 6. Use JK flip-flops. (8)

(ii) Write an HDL dataflow description of a 4-bit adder subtractor of unsigned number. Use the conditional operator (?:). (8)

12 (a) (i) For the function $F(A,B,C,D) = \sum (4,5,6,7,12,13,14)$, $d(A,B,C,D) = \sum (1,9,11,15)$ Simplify and express in SOP and in POS. (8)

(ii) Formulate a weighted binary code for the decimal digits, using weights: 6 3 1 1. (8)

(OR)

12 (b) (i) (i)Simplify the following expressions, and implement them with two-level NAND gate circuit BD+BCD′+AB′C′D′. (8)

(ii) Design a 4-bit combinational circuit 2's complementer. Show that the circuit can be constructed using exclusive-OR gates. Can you predict what the output functions are for a 5-bit 2's complementer. (8)

13 (a) (i) Implement the following Boolean function with a multiplexer:
$F(A,B,C,D) = \sum (0,1,3,4,8,9,15)$. (8)

(ii) Implement a full adder with two 4 X 1multiplexers. (8)

(OR)

13 (b) Design a four bit priority encoder with input D0 having the highest priority and input D3 the lowest priority. Develop and verify a behavioral model of the four bit priority encoder. (16)

14 (a) Design a sequential circuit with two J K Flip-flops A and B and two inputs E and x. If E = 0, the circuit remains in the same state regardless of the value of x. When E= 1 and x = 1, the circuit goes through the state transitions from 00 to 01 to 10 to 11 back to 00, and repeats. When E = 1 and x = 0, the circuit goes through the state transitions from 00 to 11 to 10 to 01 back to 00, and repeats. (16)

(OR)

14 (b) Design a 4-bit shift register with parallel load using D flip-flops. There are two control inputs: shift and load. When shift = 1, the content of the register is shifted by one position. New data is transferred into the register when load = 1 and shift = 0. If both control inputs are equal to 0, the content of the register does not change. (16)

15 (a)(i) An asynchronous sequential circuit is described by the excitation and output functions

$Y = x_1x_2' + (x_1 + x_2')y$ and $z = y$

Derive the transition table and output map and also obtain a two-state flow table. (8)

(ii) Draw the logic diagram of the product of sums expression:

$Y = (x_1 + x_2')(x_2 + x_3)$

Show that there is a static 0-hazard when x_1 and x_3 are equal to 0 and x_2 goes from 0 to 1. Find a way to remove the hazard when adding one more OR gate. (8)

(OR)

15 (b) Merge the primitive flow table that is shown below, Proceed as follows:

- Find all compatible pairs by means of an implication table
- Find the maximal compatibles by means of a merger diagram.
- Find a minimal set of compatibles that covers all the states and is closed.

	00	01	11	10
a	(a), 1	f, -	-, -	e, -
b	c, -	-, -	j, -	(b), 0
c	(c), 0	d, -	-, -	b, -
d	c, -	(d), 0	g, -	-, -
e	a, -	-, -	g, -	(e), 1
f	a, -	(f), 1	g, -	-, -
g	-, -	d, -	(g), 0	k, -
h	(h), 0	d, -	-, -	k, -
j	-, -	f, -	(j), 1	b, -
k	a, -	-, -	j, 1	(k), 0