					3	

B.E./B.TECH DEGREE EXAMINATION APR/MAY- 2011

INFORMATION TECHNOLOGY BRANCH,

THIRD SEMESTER (REGULATIONS 2008)

IT 9201 – COMPUTER ORGANIZATION

Time: Three Hours Max.Marks: 100

Answer All Questions

PART-A (10 X 2 = 20 Marks)

1. Convert the decimal number 431 to binary in two ways: Convert directly to binary; Convert first to hexadecimal and then from hexadecimal to binary. Which method is faster?
2. Express the Boolean function F=AB'+A'C as a sum of minterms. The function has three variables: A,B, and C.
3. Give the Master –Slave D flip-flop.
4. What is encoder and priority encoder?
5. Registers R1 and R2 of a computer contain the decimal values 1000 and 4000. What addressing mode is used and find the effective address of memory operand of the following instruction?
   Subtract (R1)+, R5
6. List the performance measure of a computer.
7. Compare Hardwired control Vs Micro-programmed control.
8. What is Pipelining? Give example.
9. Give the memory hierarchy.
10. What is Vectored interrupt?

PART-B (5 x 16 = 80 Marks)

11. a. i) Simplify the following Boolean expression to A) Sum-of-product
    B) Product-of-sum using Karnaugh map (8)
    ACD'+C'D+AB'+ABCD
    ii) Simplify the following Boolean function using Tabulation method and implement the simplified function using NAND gate only. (8)
    $F(w,x,y,z) = \sum (0, 1, 2, 5, 8, 10, 13)$

12. a. i) Using half-adders design a four-bit combinational circuit incrementer (A circuit that adds 1 to the four-bit binary number). (4)

ii) Implement the following Boolean function with the multiplexer. (5)
$F(A,B,C,D)=\sum(0,2,5,7,11,14)$

iii) Design a BCD –to – excess-3 code converter (7)

(OR)

b. i) A sequential circuit has 2 D flip-flops A and B, two inputs x and y, one output z is specified by the following next-state and output equations (10)

$A(t+1) = x'y + yB$

$B(t+1) = xy + y'B$

$z = B$

A) Draw the logic diagram of the circuit. (3)

B) List the state table for the sequential circuit. (4)

C) Draw the corresponding state diagram (3)

ii) With neat diagram explain the 4-bit Universal shift register (6)

13. a. i) Explain in detail the various addressing modes with example. (6)

ii) Discuss Instruction sequencing and Branching (4)

iii) Explain the non-restoring division algorithm with example. (6)

(OR)

b. i) Explain the concept behind Booth's multiplication algorithm. Multiply the following signed 2's complement numbers using the Booth's multiplication technique and Bit-pair recoding of multipliers.

A = 110011 and B=101100 (10)

ii) Write the general procedure for addition, subtraction, multiplication, and division of floating-point number. (6)

14. a. i) What is Data hazard? Explain the methods to handle Data hazard with example. (8)

ii) Explain the following methods to handle Conditional branch hazard with example
A. Delayed branch B. Dynamic branch prediction. (8)

(OR)

b. i) Explain in detail the Hard-wired control unit. (8)

ii) With neat diagram explain the multiple- bus organization. Write the sequence of control steps required for the three-bus organization for the following instruction: (8)

ADD R1, R2, R3 --- Add the contents of register R1 to register R2 and store the result in R3

15. a. i) Explain the following Memory to Cache mapping functions with example. (16)

A. Direct mapping
B. Associative-mapping
C. Four-way set-associative mapping
D. Two-way set-associative mapping

(OR)

b. i) With neat diagram explain the virtual memory organization and its address translation. (8)

ii) Discuss the Centralized and Distributed Bus arbitration. (8)