B.E / B.Tech.(Full Time) DEGREE END SEMESTER EXAMINATIONS, Nov /Dec 2012
INFORMATION TECHNOLOGY BRANCH
III SEMESTER (REGULATIONS 2008)
IT 9201 – Computer Organization

Time: 3 hrs **Max. Marks: 100**

Answer ALL Questions

Part – A (10 x 2 = 20 Marks)

1. Find the complement of (A'C+D)B+A'C'
2. Simplify the following Boolean expression to minimum number of literals
   (x+y') .(x'+y')
3. Constract a 8x1 mux using 4x1 and 2x1 mux
4. Implement following function using a 3x 8 decoder
   F(A,B,C)=A'C+BC'
5. Draw the basic block diagram of a processor
6. Explain briefly MAR and MDR . If MAR is 32 bit register and MDR is 16 bit register what should be the maximum size of memory connected to it.
7. Explain with block diagram how input output gating (R_{iin}, R_{iout}) is achieved in a register
8. Explain briefly about structural hazard in pipelining
9. Design a 1MB x 16 bit memory using 512K x 8 bit static memory chips.
10. Find the performance improvement of a system due to cache memory inclusion If a program access 110 times the memory during execution . with a cache hit rate of 90% . Assume miss penalty takes 17 clock cycles and cache access takes 1 clock cycle.

Part – B (5 x 16 = 80 Marks)

11 (i) Simplify the following Boolean function together with don't care condition and draw logic diagram (8)

$F(A,B,C,D)= \sum (0,1,2,9,14)$

$D(A,B,C,D)= \sum (8,10,15)$

(II) Design a Code converter for BCD to Excess 3 code and draw the logic diagram for it. (8)

12.a.(i) Draw and explain the working principle of a carry look ahead adder. (8)

(ii) Implement the function $F(a.b.c.d)= \sum (1,2,5,7,8,10,11,14,15)$ using 8 x 1 mux with a,b,c used as selection lines (8)

(OR)

b.i) Design a counter which counts from 0 to 5 and resets at 6 (0,1,2,3,4,5,0,1,..) (8)

ii) Draw state diagram for the given the state table , Reduce the table and draw the state diagram for that reduced state table (8)

Present state	Next state		Output	
	X=0	X=1	X=0	X=1
A	F	B	0	0
B	F	A	0	0
C	F	E	0	0
D	G	A	1	0
E	D	C	0	0
F	F	A	1	1
G	G	H	1	1
H	G	A	1	0

13, a. Simulate (1101 x 1010) multiplication using sequential circuit multiplier, draw block diagram and explain its operation

(OR)

b. Simulate the (1101 / 10) division using non restoring division with sequential circuit, draw block diagram and explain its operation

14.a. Explain in detail about the hard wired control unit and its implementation .

(OR)

b. Explain briefly about Pipelining and hazards. Discuss the techniques for minimizing data hazards

15a, Discuss in detail about cache memory, and its mapping techniques. Compare the different cache mapping techniques.

(OR)

b) Discuss about data transfer in I/O devices using interrupt and DMA techniques.