Reg. No._____

B.E./B.Tech. (FULL TIME) DEGREE EXAMINATION APRIL/MAY 2011

Eight Semester
Information Technology

IT482 – EMBEDDED SYSTEMS
(Regulation: R-2004)

Time : Three Hours Maximum: 100 Marks

Answer ALL questions
PART - A (10 x 2 = 20 Marks)

1. Compare hard real time systems with soft real time systems.
2. Define cross compiler.
3. State the typical steps inside a start up code?
4. " A pointer may have become corrupted and written into this function code space. This makes the execution to crash at this place ". Suggest a suitable solution for this problem.
5. " There is no harm in freeing a memory twice"? How and what is the reality about the statement?
6. What is "Run for ever" How it influences the ES 's memory design?
7. How interrupt latency influences the performance of an embedded system?
8. How do we pass an argument to the ISR?
9. Why Harvard architecture is preferred for ES design?
10. What happens if a lower priority task starts a higher priority task?

PART –B (5 x 16 = 80 MARKS)

11. a) Explain how stack frame is constructed for embedded systems with an example. (8)
    b) Substantiate with an example of how bottom up information from the software programming phase of design may be useful in refining the architectural design. (8)

12. a) How does heap fragmentation reduce the real time behaviour of an embedded Systems? Discuss with an example.

    (OR)

    b) What steps are taken when ISRs are called during the execution of a task? How are nested and non nested ISRs different in this regard?

13. a) For the processes and dead lines given below :
(i) Schedule the process using Rate Monotonic Scheduling (RMS)? (6)
(ii) Schedule using (Earliest Dead line First) EDF and compare the number of Context switches required for EDF and RMS (10)

PROCESS	TIME	DEAD LINE
P1	1	5
P2	1	10
P3	2	20
P4	10	50
P5	7	100

(OR)

13. b) (i) Compare Desktop OS Vs RTOS. (8)
(ii) What are the techniques that are available to tackle the problem of unbounded priority inversion. Illustrate with an example. (8)

14. a) Discuss in detail about Architecture of card verification system.

(OR)

b) Draw an UML class diagram that describes a hardware timer / counter. The device can be loaded with a count value. It can decrement the count down to zero based either on a bus signal or by counting some multiple of clock cycles.

15. a) Discuss in detail about the design of linkers and locators for embedded software with design challenges.

(OR)

b) Discuss the challenges in address resolution and locating program components for embedded software.
