Roll No.									

B.E. Degree (Full Time – Arrear) Examinations :: May – 2012

Electronics and Communication Engineering Branch

V Semester (Regulations 2004)

EC 374 – COMPUTER ARCHITECTURE AND ORGANIZATION

Time: 3 Hours Maximum Marks: 100

Answer ALL the Questions

Part – A (10 x 2 Marks = 20 Marks)

1. Draw the structure of the Turing Machine.
2. What are the limitations of Computers?
3. What are the three types of control signals have to be activated during the clock cycles in which the ADD A, B instruction is executed?
4. What are the factors determine the length of Microinstruction?
5. Draw the block diagram of serial binary adder.
6. What is meant by "Temporal Expansion"?
7. Define: Cost of Memory.
8. What are the characteristics of memory technologies?
9. Write the protocol layers of the Open Systems Interconnection reference model.
10. Draw the structure of "mesh" and "star" topologies of Bus Control.

Part – B (5 x 16 Marks = 80 Marks)

11. With neat block diagram explain the organization of a first generation computer.

12. (a). Discuss in detail about the internal structure of the data path circuit DP of a small microprocessor.

OR

12. (b). Design the control unit of the "gcd" processor using only NAND gates.

13. (a). Explain the design of carry-lookahead adder.

OR

13. (b). Explain the array implementation of the Booth Multiplication Algorithm.

14. (a). Illustrate the conceptual organization of a multilevel memory system in a computer.

OR

14. (b). With neat block diagram explain the Organization of a serial-access memory unit.

15. (a). Explain the bus arbitration scheme using "polling"

OR

15. (b). Explain the process of Direct Memory Access with neat block diagram.

***