B.E./B.TECH.(FULL-TIME) DEGREE END SEMESTER EXAMINATIONS, APRIL/MAY 2012
ELECTRONICS AND COMMUNICATION ENGINEERING
VI SEMESTER
EC 9355 DIGITAL VLSI
(Regulation 2009)

Time:3 Hrs Max Marks:100

Answer all questions

Part-A (10 X 2=20 Marks)

1) Compare between Xilinx CLB interconnect and Alter LAB interconnect.
2) Differentiate between full custom design and semi custom design.
3) Draw the stick diagram of static CMOS 2-input NAND gate.
4) For the inverter circuit shown in Fig.1 give the expression for the energy drawn from supply V_{DD} to charge capacitor C_L.

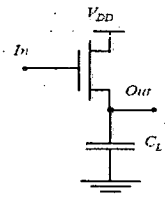

Figure 1

5) Give the logic expression for signal out in the circuit given in Fig.2.

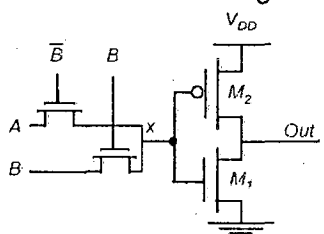

Figure 2

6) Reason out why mostly NAND gates are used to realize the combinational circuits rather than NOR gates.
7) For the memory circuit shown in Fig.3, determine the bit line values BL[0],BL[1],BL[2],BL[3], if the address is given as
WL[0]=0,WL[1]=1,WL[2]=0,WL[3]=0.

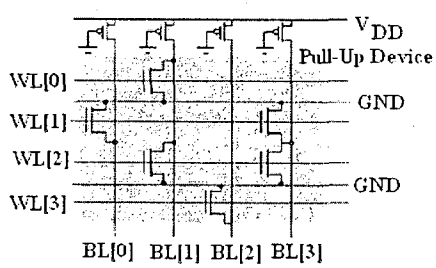

Figure 3

8) The circuit in Fig.4 shows a carry propagation path in an adder circuit. Let A, B, C_i are the inputs to adder circuit and φ is the clock signal. Write the logic expressions for the signal X, Y to generate output carry.

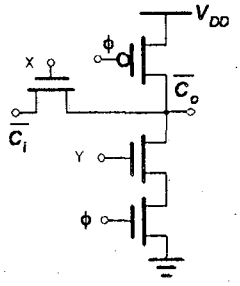

Figure 4

9) Draw a 4X4 barrel shifter.

10) List out the advantages of C^2MOS logic based register over pass-transistor logic based master-slave register.

Part-B (5 X 16=80 Marks)

11) a)i) Design 3-bit look-ahead-carry generator. Compare its performance with ripple carry adder design. (8)

ii) Design a four-bit Wallace tree multiplier. Compare its performance with four-bit carry save multiplier (8)

12. a)i) Realize the boolean logic expression Y = A'B'+C'D' in static ratioless logic style. Size the devices so that the propagation delay is equal to the delay obtained from an inverter with dimensions W/L of PMOS =3 and W/L of NMOS=1. (6)

ii) Figure 5 contains a pass-gate logic network.

x) Determine the truth table for the circuit. What logic function does it implement?

y) If the PMOS were removed, would the circuit still function correctly? Does the PMOS transistor serve any useful purpose? (4)

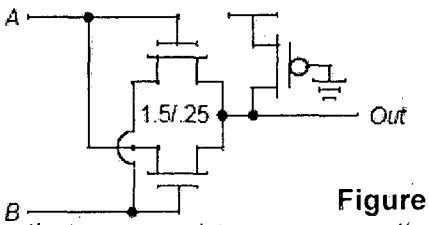

Figure 5

iii) List out the techniques that are used to overcome the degradation of NMOS pass transistor logic. Elaborately discuss any one technique (6)

(OR)

b) i) Implement the equation $X = \overline{(A+B)CD}$ using complementary CMOS logic.

x) Size the devices so that the output resistance is the same as that of an inverter with an NMOS W/L = 4 and PMOS W/L = 8.

y) What are the input patterns that give the worst case *tpHL* and *tpLH*. Consider the effect of the capacitances at the internal nodes.

z) If P(A=1)=0.2, P(B=1)=0.5, P(C=1)=0.1, P(D=1)=1, determine the power dissipation in the logic gate. Assume VDD=1.8V, Cout=150fF and fclk=550MHz. (10)

ii) Implement the logic function $Y= \overline{(A+B.(C+D))}$ using dynamic CMOS logic. (2)

iii) List out the signal integrity issues in dynamic CMOS logic design and explain any one of the issue in detail. (4)

13) a)i) Analyze the impact of spatial and temporal variations of clock signal on edge-triggered sequential logic circuits. (8)

ii) Design a positive edge trigger register in TSPC logic. Compare TSPC logic with C^2MOS logic. (8)

(OR)

b)i) Consider the circuit shown in Fig.6.

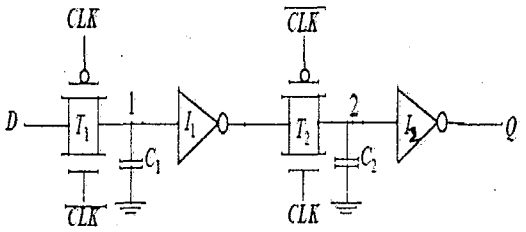

Figure 6

(x)State whether the circuit is a latch or edge triggered register. Justify your answer.

(y)In the circuit consider C1 and C2 as the intrinsic capacitances of inverters and transmission gates. Assuming ideal clock, compute the setup time, hold time and propagation delay in terms of the inverter I1, I2 delay and transmission gate T1, T2 delay. (6)

ii) Construct 3T based DRAM cell. Explain its read and write operations with the help of signal waveforms. List out the advantages of 3T based DRAM cell over 1T based DRAM cell. (10)

14) a)i) Briefly describe the ASIC design flow with the help of a flowchart. (8)

ii) Explain the CLB of Xilinx XC4000 in detail. (8)

(OR)

b)i) Realize the function, F=A.B+(B'C)+D using ACTEL- FPGA. (6)

ii) Explain the Altera MAX 7000 architecture in detail. (10)

15) a)i) Explain the manufacturing process of CMOS with necessary diagrams. (12)

ii) Determine the change in threshold voltage of NMOS transistor due to body effect. Let $N_A=3X10^{16}$, ni= $1.5X10^{10}$, tox=200Å, $V_{TO}=0.4V$ and VSB=2.5V. (4)

(OR)

b)i) List out the goals of CMOS technology scaling. Explain any two methods in detail (10)

ii) Derive the expression to obtain the minimum delay through the chain of CMOS inverter. (6)