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UNIVERSITY DEPARTMENTS, ANNA UNIVERSITY – CHENNAI
DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

B.E. DEGREE EXAMINATIONS, APRIL 2011

III SEMESTER – R 2008

CS 9204 COMPUTER ARCHITECTURE

Time: Three Hours Max. Marks: 100

Answer All Questions

PART-A (10 X 2 = 20 Marks)

1. Consider a load-store processor with a clock cycle time of 1 ns. running a program with the following instruction mix :

	Frequency	Clock cycle count
ALU operations	50%	1
Loads	20%	3
Stores	10%	3
Branches	20%	2

A second level of cache is being added, that speeds up memory access time by 2, and increases clock cycle time by 30%. Find the improvement obtained.

2. Discuss the concept of a carry look ahead adder.

3. Discuss the features to be considered while deciding on the choice of addressing modes.

4. What is a control store? Discuss.

5. What is meant by static branch prediction?

6. Discuss the concept of loop unrolling by the compiler.

7. What is a TLB? Discuss.

8. What is a write buffer?

9. What are the functions to be performed by an I/O interface?

10. What is daisy chaining?

PART-B (5 x 16 = 80 Marks)

11. (i) Discuss the basic steps involved in the instruction cycle of a processor. Show the sequence of operations that take place in a single bus organization for the instruction
ADD ADDR, R2, # DATA
where the format is ADD dst, src1, src2. (10)

(ii) Discuss the concept of microprogramming. How does it compare with hardwired control? (6)

12. a. (i) Discuss the construction of a 4x4 array multiplier. (10)

(ii) What is a carry save adder? What are its advantages? (6)

OR

b. (i) Discuss the restoring division algorithm.
Simulate the same for the numbers 15 / 9. (10)

(ii) Discuss the operation of a floating point adder/subtractor unit. (6)

13. a. (i) Discuss the book keeping done by the Tomasulo's dynamic scheduling algorithm.

Schedule the following code assuming that the hardware has one integer unit (handles also all memory references and branches) with a 1-cycle execution latency, one Floating-Point Add/Sub unit with 2-cycles execution latency, two FP Mult units with an execution latency of 10 cycles, and one FP Div unit with a 40-cycle latency. (10)

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LD      F6  34(R2)
LD      F2  45(R3)
MULD    F0, F2, F4
SUBD    F8, F0, F2
DIVD    F10, F0, F6
ADDD    F6, F10, F2
MULD    F2, F0, F6
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(ii) What is meant by delayed branching? Discuss the different ways by which the compiler fills the branch delay slots. (6)

OR

b. (i) Discuss the implementation of the MIPS integer pipeline. What are the additional complexities to be handled in a floating-point pipeline? (10)

(ii) What is meant by hardware speculation? How is it handled in a dynamically scheduled processor? (6)

14.a. (i) Compare and contrast the various mapping policies used in cache memories.

A computer system has a main memory consisting of 16M words. It also has a 4K-word cache organized in the block-set-associative manner, with 4 blocks per set and 128 words per block.
Calculate the number of bits in each of the TAG, SET and WORD fields of the main memory address format. (10)

(ii) Discuss any four techniques used for improving the performance of the cache. (6)

OR

b. (i) What are the advantages of virtual memory?
Show how a paged memory management technique is implemented. (10)

(ii) What is the need for a hierarchical memory system?
Show the complete flow of data between the processor and memory, assuming there are two levels of cache and support for virtual memory. (6)

15.a. (i) What is the need for a DMA transfer in a computer system?
Discuss in detail how this is accomplished. (10)

(ii) Distinguish between synchronous and asynchronous bus transfers. (6)

OR

b. (i) What is the need for standard I/O interfaces?
Discuss in detail any one standard interface. (10)

(ii) What is an interrupt driven transfer? Discuss. (6)

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