Roll No. | | | | | | | | | | |

B.E / B.Tech (FT) END SEMESTER EXAMINATIONS – APRIL / MAY 2019

COMPUTER SCIENCE AND ENGINEERING

Semester 2

CS8201 DIGITAL PRINCIPLES AND SYSTEM DESIGN
(Regulation 2012)

Time: 3 Hours | Answer ALL Questions | Max. Marks 100

PART-A (10 x 2 = 20 Marks)

1. Draw logic diagram to implement the boolean expression F= (w'+x')(y'+z).
2. Prove the identity of the following Boolean function using algebraic manipulation. Clearly indicate the postulates and theorems used.
   ab + a'c + bc = ab + a'c
3. Design a full adder using half adders.
4. Define decoder.
5. What is mealy model?
6. Write a verilog module for SR flip-flop.
7. What is critical race condition in asynchronous sequential circuit?
8. Determine the maximal compatibles for the following compatible pairs using merger diagram. (a, b)(d, e)(d, g)(e, g)
9. Draw the logic diagram of the memory cell.
10. What is memory decoding in digital design?

Part – B (5 x 16 = 80 marks)
(Question No.11 is Compulsory)

11. i. Design a two's complementer circuit using T flip flop (10)
    ii. Design a XOR and AND gate using NOR gate (6)

12. a) i. Simplify the following Boolean function F1 by means of Karnaugh map and implement using NAND gates. (10)
    F1 (A, B, C, D) = Σm (0,1,4,5,8,9,10,12,13)
    ii. Write and verify the verilog model of the circuit. (6)

    (OR)

    b) i. Design a four line to two line priority encoder with input D0 having the highest priority and input D3 the lowest priority. (10)
    ii. Write and verify the verilog model of the circuit. (6).

13. a) Design a 3-bit binary counter with 3, 7 as unused states using T flip-flop. Write a verilog module of the circuit.

    (OR)

    b) Design and describe a 4-bit universal shift register? Write a structural HDL code for 4-bit universal shift register.

14. a) Derive the Boolean function for the outputs of two SR latches Y_1 and Y_2 of an Asynchronous sequential circuit shown in Figure 1. Derive the transition table and output map of the circuit.

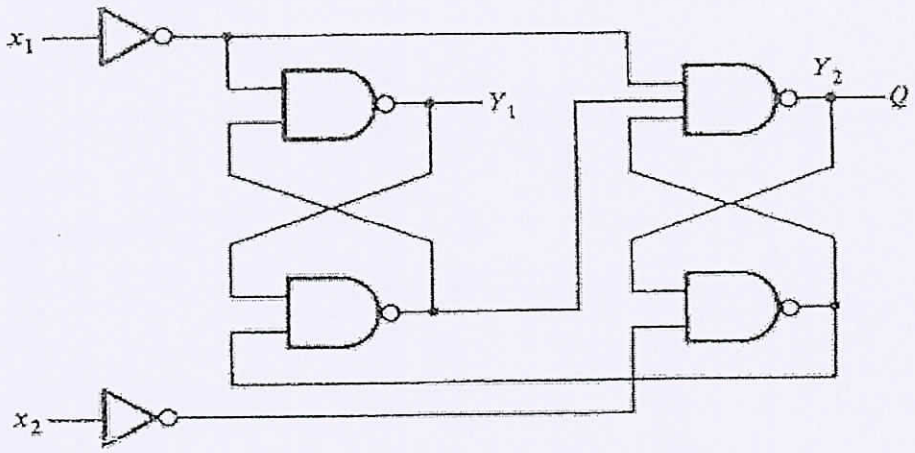

Figure 1. Asynchronous sequential circuit

(OR)

b) Design a gated latch circuit with two inputs, G (gate) and D (data), and one output Q. Binary information present at the D input is transferred to the Q output when G is equal to 1. The Q output will follow the D input as long as G = 1. When G goes to 0, the information that was present at the D input at the time the transition occurred is retained at the Q output. The gated latch is a memory element that accepts the value of D when G = 1 and retains this value after G goes to 0. Once G = 0, a change in D does not change the value of the output Q. Simultaneous transition of two input variables are not allowed. Obtain the primitive flow table, reduction of the primitive flow table and logic diagram.

15. a) i. Explain about the three major types of sequential programmable device with example. (10)

ii. Write a verilog module for the operation of memory unit that has 64 words of four bit each. (6)

(OR)

b) i. Consider an even parity hamming code 1100010 is received at the receiver side. Check if any error occurs then determine the error bit location and correct the error. (10)

ii. Design a PAL circuit to implement the 3 bit binary-gray code conversion.(6)