B.E (Full Time) - END SEMESTER EXAMINATIONS APRIL / MAY 2019
ELECTRONICS AND COMMUNICATION ENGINEERING
3rd SEMESTER
EC 8351 DIGITAL ELECTRONICS AND SYSTEM DESIGN
(Regulation 2012)

Time: 3 Hours | Answer ALL Questions | Max. Marks 100

PART-A (10 x 2 = 20 Marks)

1. Convert BEA_{16} to octal.
2. Express F=xy + x'z as a product of maxterms.
3. Draw the schematic of a 4 to 1 mux.
4. Draw the circuit of a full adder using two half-adders and an OR-gate.
5. Write all the states possible in a 4-bit Johnson counter.
6. What is lock out in counters?
7. Mention two problems in asynchronous sequential circuits.
8. Define static-0 hazard?
9. Define fan out.
10. Draw the circuit of a CMOS inverter.

PART-B (5 x 16 = 80 Marks)

11. Obtain simplified SOP using Quine McCluskey / tabulation method for **F(a,b,c,d)=Σ(** (0,3,5,6,7,10,12,13)

12a) Design a combinational circuit with three inputs, x , y and z and three outputs, A, B and C . When the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is two less than the input. Realize the circuit using an appropriate decoder.

OR

12b) Design a 3-bit binary to 2s complement converter. Realize using an appropriate decoder.

(PTO)

13a) Design a synchronous sequential counter with states 0,6,7,4,5,2,3,1,0,6….. repeat using JK FFs.

OR

13b) Obtain the state table and state diagram for a circuit consisting of two T FFs, an external input, x, and output, y, described by the equations $T_A=Q_B x$, TB=x and $y=Q_A Q_B$.

14a) Obtain a reduced pft for an async. seq. circuit with two inputs A and B and one output Z where Z changes whenever AB=11. Assume that the two inputs do not change simultaneously and initial Z=0.

OR

14b) Explain essential hazard with an example.

15a) Explain the working of a TTL tristate gate.

OR

15b) Explain the working of 2-input CMOS NAND and NOR gates.

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