14/05/19

Roll No. | | | | | | | | | | |

B.E./B.Tech/ B.Arch (Full Time) END SEMESTER EXAMINATIONS, APRIL/MAY 2019

ELECTRONICS AND COMMUNICATION ENGINEERING BRANCH

SEVENTH SEMESTER

EC 8005 – CAD for VLSI

(REGULATIONS 2012)

Time: 3 Hours | Max. Marks: 100

Answer ALL Questions

PART-A (10 x 2 = 20 Marks)

1. Draw Gajski's Y chart.
2. Define the minimum spanning trees?
3. List out the applications of Layout compaction.
4. Draw a clique model for RS latch.
5. List the optimization problems related to floor planning.
6. Distinguish between area routing and channel routing?
7. List the types of delay modeling.
8. Represent the Boolean function Y = A (B + C) as a binary decision diagram.
9. Gives the rule for selector node and distributor node in DFG.
10. Why allocation and scheduling are to be considered in high level synthesis?

Part – B (5 x 16 = 80 marks)

11. i) Explain various steps involved in the VLSI design process clearly indicating the various CAD tools used.

ii) Using Prim's algorithm, find the minimum spanning tree for the graph shown in figure

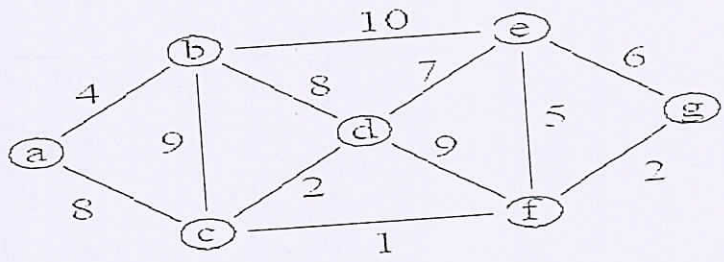

Figure 1

12.a)i) Explain briefly about placement Algorithm. (8)

ii) Discuss about the constraint-graph for Liao-wong Algorithm. (8)

(OR)

b)i) Describe in detail about Bellman-Ford algorithm. (8)

ii) Find the minimum cut cost for the initial partitioning of a following figure 2 by using Kernighan-Lin algorithm? (8)

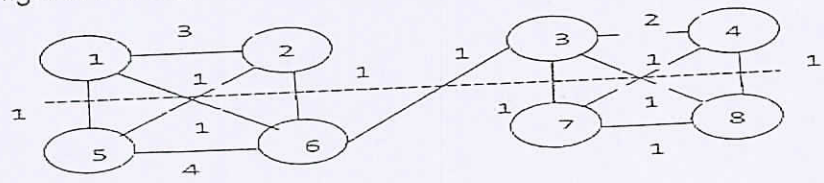

Figure 2

13.a)i) Draw vertical and horizontal polar graphs for the slicing floor plan for the figure 3 (8)

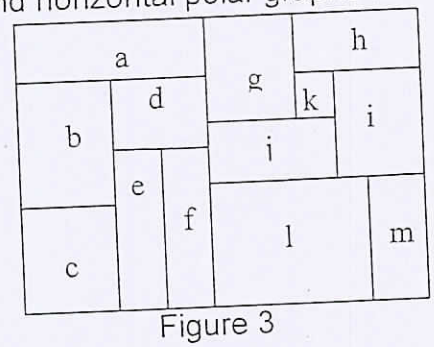

Figure 3

(ii) Discuss the shape function and floor planning sizing? (8)

(OR)

b) Explain the basic version of Lee's algorithm for area routing. (16)

14.a)i) Write short notes on Gate-level modeling. (8)

ii) List and explain the steps involved in two level logic optimization. (8)

(OR)

b) To implement the following Boolean equation (16)

$G = x_1.\overline{x_2}$ by using robdd _ build function. Compute compliment function of G..

15.a)i) Explain the register assignment for the second order DFG filter. (8)

ii) Explain the list scheduling Algorithm with Example. (8)

(OR)

b) Draw the structure of the different hardware components used by a high- level synthesis system. (16)