15/05/19

Roll No. | | | | | | | | | | |

B.E (FT) END SEMESTER EXAMINATIONS – APRIL / MAY 2019

ELECTRONICS AND COMMUNICATION ENGINEERING

6th Semester

EC8011 EMBEDDED AND REALTIME SYSTEMS

(Regulation 2012)

Time: 3 Hours | Answer ALL Questions | Max. Marks 100

PART-A (10 x 2 = 20 Marks)

1. At what stage of the design methodology would we test our design for functional correctness?
2. Differentiate between big-endian and little-endian representation.
3. Draw a UML sequence diagram for a busy-wait read of a device. The diagram should include the program running on the CPU and the device.
4. If an interrupt handler executes for too long and the next interrupt occurs before the last call to the handler has finished, what happens?
5. Bring out the difference between an interpreter and JIT compiler.
6. What is meant by four cycle handshaking protocol?
7. Name an embedded system that requires both periodic and aperiodic computation.
8. List out the functionalities of RTOS.
9. What is the data transfer rate supported by Myrinet?
10. What is the necessity for a multiprocessor environment in embedded system design?

PART-B (5 x 16 = 80 Marks)

11.a) Draw the dataflow core model of an ARM processor and explain its functional blocks. Also mention about the various operating modes supported by the ARM processor (16)

(P.T.O)

12.a)(i) Draw a UML sequence diagram for copying characters from an input to an output device using busy wait I/O. The diagram should include the two devices and two busy-wait I/O handlers. (8)

(ii) With a neat block diagram and timing diagram, explain how data transfer takes place using direct memory access (DMA)? (8)

(OR)

12.b)(i) With neat diagram, explain in detail about the ARM address translation scheme. (8)

(ii) Bring out the difference between a timer and counter circuits and how are they designed? (8)

13.a) With relevant examples, briefly explain the various loop transformation techniques. (16)

(OR)

13.b) With suitable examples, explain briefly about the various methods used in clear box testing and black box testing. (16)

14.a) Consider the following system of periodic processes executing on a single CPU:

Process	CPU Time	Deadline
P1	4	200
P2	1	10
P3	2	40
P4	6	50

Can we add another instance of P1 to the system and still meet all the deadlines using RMS? (16)

(OR)

14.b) With neat sketches, explain in detail about the interprocess communication mechanism (16)

15.a) With relevant diagrams, explain briefly on how an I^2C bus is used for performing data transfer. (16)

(OR)

15.b)(i) With neat sketches, briefly explain the working of a SHARC link port. (8)

(ii) With an example, explain how does a single threaded or multithreaded control of an accelerator will affect the speedup factor. (8)