17/05/19 (AN)

B.E /B.Tech (Full Time) END SEMESTER EXAMINATIONS, MAY 2019
ELECTRONICS AND COMMUNICATION ENGINEERING
THIRD SEMESTER
EC8301 ELECTRONIC CIRCUIT -1
REGULATION(R-2012)

Time: 3 Hours | Max. : 100marks

Answer All Questions

PART-A (10 X 5=20(Marks)

1.Draw a Fixed bias circuit of BJT and design the value of Rc and R_B ,given Vcc=20V,β= 200 , I_{CQ}=1 μA and V_{CQ}=8 V

2.Mention the different biasing methods for JFET.

3.Write any two important features of Darlington Amplifier

4.In a NMOS device V_A=50V and I_{DQ}= 2mA.Calculate the value of ro of the device and the channel length modulation factor.

5.Draw the equivalent circuit of CS amplifier .

6.Compare the voltage gain of CB and CC amplifier

7. Mention the low and high frequency capacitors of a MOSFET amplifiers.

8. Define f_T of CE amplifier.

9 Draw CD NMOS amplifier with active load

10.What is meant by channel length modulation.

PART-B (16X5=80 marks)

11(i). Explain compensation methods for stabilizing I_C with respect to V_{BE} and I_{CO} (reverse saturation current) (8)

(ii) Derive for the stability factor S of a Self bias circuit of BJT. (8)

12 .(a) Draw a CC BJT amplifier and its equivalent circuit. Derive for A_v, A_I, R_{in} and R_0

(OR)

(b) Draw a cascode Amplifier and with equivalent circuit derive for R_{in}, R_0, A_I and A_V.

13.(a) Derive the voltage gain of BiMOS cascode amplifier shown in Fig 1

(OR)

(b) Draw a discrete Common Gate JFET amplifier and derive Voltage gain Av,A_I ,Input impedance R_{in} and Output impedance R_{out} with small signal equivalent circuit.

14 .(a) (i) Derive fα and fβ with equivalent circuit. (10)

(ii) What is meant by Miller's capacitance and what is the effect of Miller's capacitance in CE amplifiers. (6)

(OR)

(b)(i) Define and derive expressions for f_T of MOSFET (6)

(ii)Consider the common-gate circuit in Fig 2 with parameters $V+$ =5 V, $V-$ = −5 V, R_S=4K, R_D= 2 K, R_L= 4K, R_G= 50K, and Ri= 0.5K. The transistor parameters are: K_p= 1mA/V^2, V_{tp}=−0.8 V, $\lambda = 0$, C_{gs}= 4 pF, and C_{gd}= 1 pF. Determine the upper 3 dB frequency and midband voltage gain. (10)

15.(a) Draw a CMOS differential amplifier using NMOS driver and PMOS current source as active load and with its equivalent circuit derive for A_D ana A_C .

(OR)

(b)(i)The circuit to be designed has the configuration shown in Fig 3. The bias voltages are (4)
$V+ = 5$ V and $V- = 0$. Transistors are available with parameters $kn = 40\ \mu A/V^2$, $VTN = 1V$, and $\lambda = 0$. Design the circuit such that $IREF = 0.35mA$, $IO = 0.20mA$, and $VDS2(sat) = 0.85$ V.)

(ii)Draw a CMOS CS amplifier and derive for Av (6)

(iii)Draw a MOS current steering circuit and explain (6)

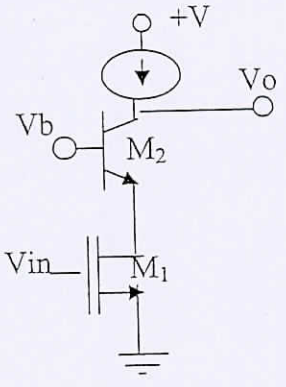

FIG 1

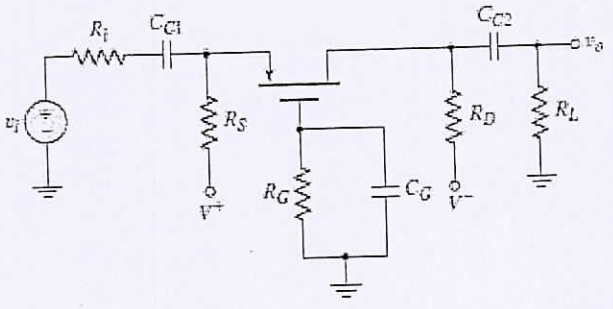

FIG 2

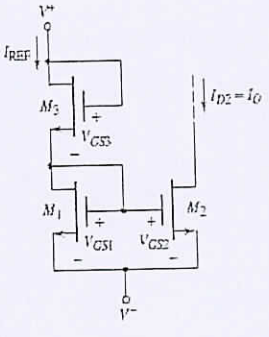

FIG 3