B.E./B.Tech. (FT) DEGREE END SEMESTER EXAMINATIONS, APR/MAY 2019

Branch: Electronics and Communication Engineering

Fourth Semester

EC 8451 - Computer Architecture and Organization

Regulations 2012

Time: 3 Hours Max.Marks: 100

Answer ALL the Questions

PART – A (10 x 2 Marks = 20 Marks)

1. How do you represent a negative numbers when designing an ALU?
2. What are the four basic types of operations performed by any instruction set?
3. Draw the data path required to implement 4 bit addition
4. How do you detect the overflow in 2's complement addition?
5. What is the speedup ratio of a pipeline over a non-pipelined machine?
6. Compare and contrast Hard-wired control unit and Micro-programmed Control unit
7. Define Address space and Memory space
8. Why do we prefer Associative memory for constructing the cache?
9. What do you meant by Handshake method of Data Transfer?
10. Why do we need Interrupt?

PART – B (5X16 = 80 Marks)

11 Explain any eight addressing modes used in Computer Architecture with examples

12(a) With a neat flow chart, explain addition and subtraction of floating point numbers

OR

12 (b) Draw the circuit diagram fir a 4-bit Ripple Carry Adder and explain how the delay time is reduced in the 4-bit Ripple Carry Look Ahead Adder.

13 (a) Explain the control points for a multiplier, and also design a micro-programmed control unit for this multiplier

OR

13 (b) Discuss the occurrences of hazards in a pipeline and explain the mechanism used for overcoming these hazards

14 (a) Explain the various mapping schemes used in cache design. Compare the schemes in terms of cost and performance.

OR

14 (b) Discuss the concept of virtual memory and explain how virtual address is converted into physical address with a neat diagram.

15(a) With a neat diagram, explain Vectored Interrupt and DMA

OR

15(b) Write Short notes on

(i) CISC Processors

(ii) RISC Processor

(iii) Superscalar Processor

(iv) Vector Processor

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