Roll No. | | | | | | | | | | |

FULL

B.E / B.Tech (~~Part~~ Time) Degree End Semester Examinations, April / May 2019

Department of Electronics and Communication Engineering

EC8651 DIGITAL VLSI

(Regulations: 2012)

Time: 3 Hours | Answer ALL Questions | Max. Marks 100

PART-A (10 x 2 = 20 Marks)

1. Determine the regions of operation of MOS transistor for V_{T0}=0.4 V, V_{GS}= 1.5 V, V_{DS}=2.0 V and V_{T0}= - 1 V, V_{GS}= - 1.5 V, V_{DS} = -2.0 V.
2. Define full scaling.
3. Calculate the switching activity, $\alpha_{0\to1}$, for a 2-input NAND gate given $p_{(A=1)}$ = 0.2 and $p_{(B=1)}$ = 0.1.
4. Determine the logical effort of two input dynamic NOR gate assuming PMOS-NMOS ratio of 2 in the minimum sized inverter.
5. What are the time constraints required to overcome race conditions in dyanamic registers.
6. Implement AND logic using TSPC approach.
7. Write the delay expression for carry save multiplier.
8. Draw the Mirror adder circuit.
9. What is semi custom design.
10. What is cell based ASIC.

Part – B (5 x 16 = 80 marks)
(Question No.11 is Compulsory)

11 i) Derive the expressions for drain current of MOS transistor for various regions of operation. (8)

ii) Determine the required ratio of PMOS to NMOS transistor sizes such that the switching threshold of CMOS inverter is set to desired value of V_M= 1.25 V for V_{DD}= 2.5 V. Assume the following device parameters for design calculation. (8)

NMOS: K'_n=115μA/V^2 ,V_{t0}=0.43V, λ_n = 0.06V^{-1}, V_{DSAT}=0.63V
PMOS: K'_p =-30μA/V^2,Vt_0=-0.4V, λ_p = - 0.1V^{-1}, V_{DSAT}= -1V

12 a.i) Implement F = $\overline{(A+B)C + D}$ using static CMOS logic. Size the devices so that the output resistance is the same as that of an inverter with $(W/L)_n$ = 1 and $(W/L)_p$ = 4. (8)

ii) Describe the implementation of pseudo-NMOS inverter and derive the parameters V_{OL} and P_{low}. (8)

(OR)

b.i) Implement AND/NAND and XOR/ XNOR gates using complementary pass transistor logic. (8)

ii) Explain the signal integrity issues in dynamic design. (8)

13 a.i) Describe the implementation of multiplexer based master-slave positive edge triggered register.and its timing properties. (8)

ii) Implement 4 X 4 MOS NOR and NAND ROM to store the values 1011, 0110, 0101 and 1001. (8)

(OR)

b.i) Explain how the implementation of C^2MOS master-slave positive edge triggered register is insensitive to clock overlap. (8)

ii) Describe the write operation of 6T SRAM cell and derive pull up ratio. (8)

14 a.i) Explain with appropriate expressions the implementation of carry look ahead adder. (8)

ii) Draw the block diagram of 4 bit array multiplier and derive its delay. (8)

(OR)

b.i) Describe the implementation of 16 bit square root carry select adder and derive its propagation delay. (8)

ii) Draw the block diagram of 4 bit Wallace multiplier and derive its delay. (8)

15 a) Explain with appropriate diagram any one type of FPGA logic cells and corresponding interconnect architecture.

(OR)

b). Explain different types of gate array based ICs.