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B.E ( Full Time ) DEGREE END SEMESTER EXAMINATIONS, APRIL/MAY 2019

ELECTRICAL & ELECTRONICS ENGINEERING

EE 8301 Digital Systems

(Third semester)

(Regulation 2012)

Time:3 hours Part-A (10x2=20) Answer ALL Questions Max Marks:100

1. Determine the base 'b' in each of the following cases : (i) $(361)_{10} = (551)_b$ (ii) $(859)_{10} = (5B7)_b$
2. Write the 8-bit signed magnitude, 2's compliment and 1's compliment form of the decimal number (-13)
3. Using the theorems of Boolean algebra simplify the following Boolean expression.f1(A,B,C,D) = B+BCD+B'CD+AB+A'B+B'C
4. Express the three-variable function $f(A,B,C)=\sum m(0,1)$ as a product of max terms
5. A combinational circuit is described by the equations $f_1(A,B,C)=ABC + A'B'C$ $f_2(A,BC) = A'B'C' + A'BC$ ; Design a circuit which will implement these two equations using a decoder with an AND gate external to the decoder.
6. Implement the following four variable Boolean function using four input multiplexers and NAND gates.$f(A,B,C,D) = \Sigma m(0,7,8,9,10,11,15)$ Use B and C as control variables.
7. Give the truth table and excitation table of SR Flip Flop.
8. Draw the circuit diagram of three bit up-counting ripple counter
9. Differentiate asynchronous and synchronous circuits.
10. Differentiate combinational logic and sequential logic circuits.

Part-B 5 x 16 =80

11 (i)Design a three bit synchronous counter that goes through the following states 1,2,4,6,0... use T FFs for realisation. (12)

(ii)Design a four bit binary down counter(ripple) (4)

12.(a)(i) Design a full adder circuit. (8)

(ii) Reduce the Boolean function $f(A,B,C,D) = \sum (0,1,2,3,4,8,10,12,14)$ using Karnaugh map and implement using gates. (8)

(OR)

12(b) Design a BCD to 2421 code converter using AND,OR and Invert gates.

13(a) (i)Implement the following 4-variable functions using 3 x 8 decoders having active low outputs and NAND gates:

$f_1 = \sum m( 0, 1, 3,9, 12, 14)$

$f_2 = \sum m( 5, 9, 12, 13, 15)$

$f_3 = \pi M (0 3, 8,11,12,15)$

$f_4 = \pi M( 1,2, 7, 8,11,12,14)$ (8)

(ii) Construct a 5X32 decoder with four 3 x 8 decoders with enable inputs and one 2 x 4 decoder. (4)

(iii)Draw the internal circuit diagram of a 8 x 1 multiplexer and give the truth table. (8)

(OR)

13(b)(i) Implement the following 4-variable Boolean function using 4-input multiplexers and NAND gates: $f(A,B,C,D)=\sum m( 0, 1, 3, 5, 6, 8, 9, 11, 12, 13)$ control variables A and B(6)

(ii) Give a brief description about PAL (4)

(iii) Implement the following 4-variable functions using a 16 x 4 ROM:

$f_1 = \sum m(0, 1, 3, 9, 12, 14)$

$f_2 = \sum m(5, 9, 10, 12, 13, 15)$

$f_3 = \sum m(0\ 3, 8, 11, 12, 15)$

$f_4 = \sum m(1, 2, 7, 8, 11, 12, 14)$ (6)

14 (a) For the sequential network shown in figure-1, derive the state table and draw the state diagram. What is the function of the circuit? (16)

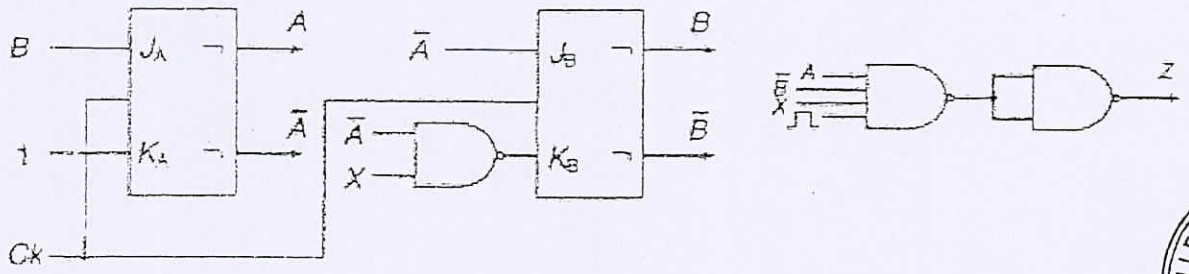


Figure 1



(OR)

14.b) Design a synchronous counter that goes through the sequence ...2,3,7,9,10,12,2.... Use JK FFs for implementation. (16)

15(a) Design a synchronous modulo-11 counter using NAND gates and T flip-flops

(OR)

15(b) Analyse the circuit shown in Figure-2

(i) Determine the state table.

(ii) Determine the state diagram.

(iii) Use the state table to determine the output response to the input sequence X1X2 = 00, 01, 11, 10, 00, 01, 11, 01, 11, 10, 00.
Assume the initial conditionsare X1 = X2 = 0 and A = B =0.

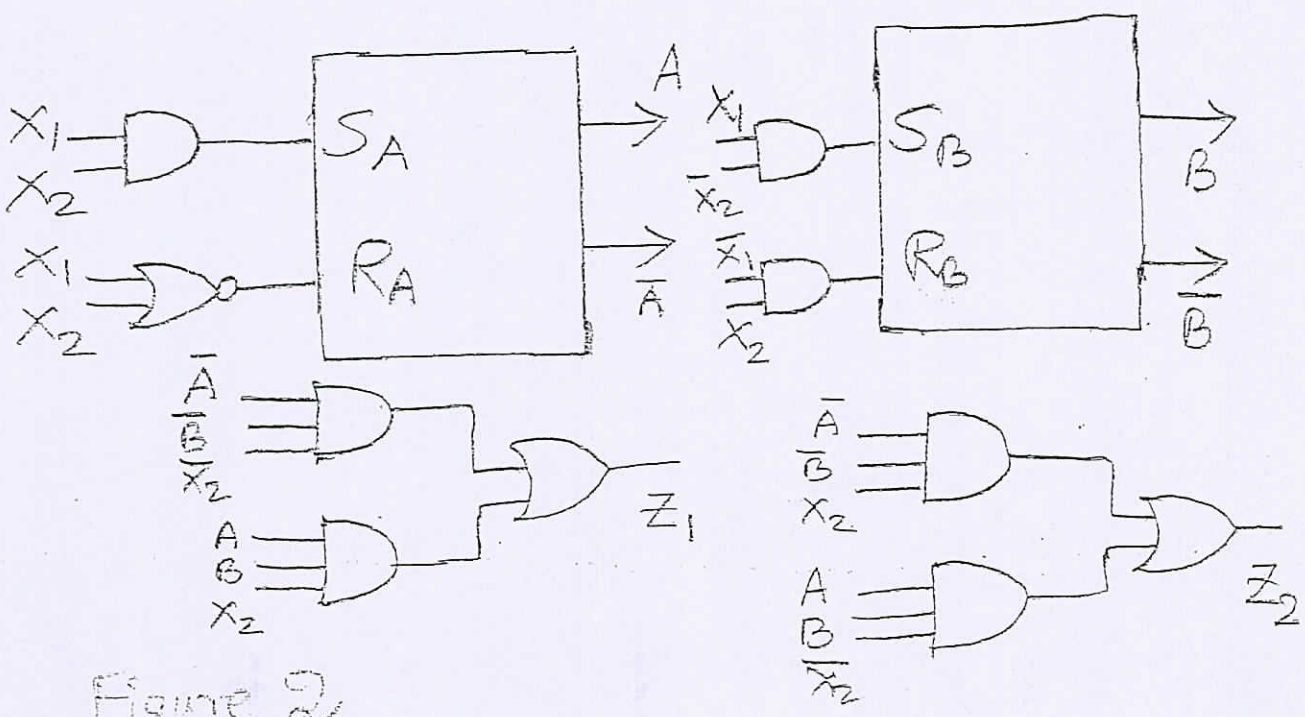


Figure 2