16/05/19

B.E / B.Tech.(Full Time) DEGREE END SEMESTER EXAMINATIONS, APR/MAY 2019
INFORMATION TECHNOLOGY BRANCH
III SEMESTER (REGULATIONS 2012)
IT 8301 – Computer Organization

Time: 3 hrs Max. Marks: 100

Answer ALL Questions

Part – A (10 x 2 = 20 Marks)

1. Simplify using Boolean algebra (BC' +A'B) (BC' +ABC'+A'B)
2. Convert 64 into binary, octal and Hexa decimal number
3. Design a 2 bit Comparator circuit
4. Design a 3 bit up counter using T flip flop
5. Discuss briefly about performance equation of a system
6. Discuss about direct and indirect addressing mode with example
7. Write instruction sequence for C=A+B statement
8. Explain briefly data hazard in pipelining
9. Discuss need for virtual memory
10. Explain briefly programmed I/O

Part – B (5 x 16 = 80 Marks)

11 (i) Simplify the following Boolean function using K-map with don't care condition and draw logic diagram and give truth table (8)

$F(A,B,C,D)= \sum (0,1,2,3,7,9,10,15)$
$D(A,B,C,D)= \sum (4,5,8,11,12)$

(ii) Represent the following in SOP and POS form (8)
F(x,y,z) = xy' + x'y+xz'

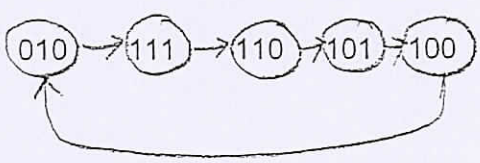
12.a (i) Implement the following function using 8x 1 MUX and B,C,D as selection lines
$F(A,B,C,D) = \sum (1,2,6,8,12,14)$ (8)

.(ii) Explain the operation of 3 x 8 decoder and its uses. Implement the function using 3x8 decoder and draw logic diagram (8)
F(A,B,C)= A'BC+BC'+AC'+A'BC'

(OR)

b.i) Differentiate PAL and PLA with implementing F(A,B,C)=ABC+A'B'C+ABC' (8)

ii) Design a 3 bit binary counter using T Flipflop Show state table (8)



13, a. Simulate (1010 % 101) with non-restoring division using sequential circuit binary divider. Draw block diagram and explain operation of sequential circuit binary divider

(OR)

b. Explain in detail Floating point processor for performing addition/subtraction operation

14.a. Explain in detail about the hardwired control unit and its implementation. Explain advantage and disadvantage of hardwired control unit

(OR)

b. Explain briefly about instruction hazard. Discuss the techniques for minimizing instruction hazard

15a. Discuss in detail about memory mapping technique of cache memory with diagram and example

(OR)

b. Discuss about DMA controller and its operation in data transfer