B.E (FT) END SEMESTER ARREAR EXAMINATIONS – NOV / DEC 2023

Computer Science and Engineering

Fourth Semester

CS6107 – COMPUTER ARCHITECTURE

(Regulation 2018 - RUSA)

Time: 3 Hours | Answer ALL Questions | Max. Marks 100

Note: Assume data, if required

PART-A (10 x 2 = 20 Marks)

1.	Specify the instruction format for R type instruction, give example.	2
2.	What are condition codes? How are they used?	2
3.	Illustrate how jump address is computed.	2
4.	Discuss the following instruction of MIPS: beq, addi	2
5.	Design a 8 bit adder using full adders.	2
6.	Apply bit pair recoding on the multiplier 100001110.	2
7.	State the principle behind loop unrolling.	2
8.	Discuss the concept of (m,n) predictorwith an example.	2
9.	How do we accomplish memory interleaving?	2
10.	DMA results in cycle stealing? Why is it called so?	2

PART – B (8 x 8 = 64 marks)

(Answer any 8 questions)

11.	State the processor performance equation I. Discuss in detail the influence of various parameters and derive performance equation II.	8
12.	Write a MIPS assembly language program to find the total ofthe given five marks stored in an array.	8
13.	Explain how subroutines are handled in MIPS architecture. Illustrate with a subroutine to find the given number is prime.	8
14.	Summarize the different addressing modes used in MIPS architecture and explain the address computation with example.	8
15.	State and explain Booth's algorithm. Simulate Booth's algorithm to find -5*6.	8

16.	Illustrate the division algorithm with a sequential circuit and flowchart. Simulate it for 11/3	8
17.	Explain the working of floating point addition with a circuit and flowchart.	8
18.	Draw the data path for lw $s0, 4($s1) and explain.	8
19.	Explain the control signals generated byALU control unit and also tabulate the description for the possible states of the control signals	8
20.	Elaborate the different cache mapping techniques. Illustrate the mapping techniques with suitable examples. Draw the implementation of 2-way set-associative cache with a cache of size 1K blocks.	8
21.	Explain the concept of virtual memory. Explain how address translation is made faster using TLB.	8
22.	Describe the working of I/O transfer where processor is relieved with neat illustration.	8
	PART – C (2 x 8 = 16marks)	
23.	Discuss in detail the dynamic branch prediction strategies with necessary illustrations.	8

24.	Identify the dependencies and hazards in the following code sequence. Also suggest solutions for the hazards identified.
	LD R1, 0(R3)
	SUB R4, R1, R3
	LD R4, 32(R5)
	ADD R1, R1, R4
	SUB R3, R4, R2
	LD R4, 32(R3)
	SD R4, 50(R1)
		8