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ANNA UNIVERSITY (UNIVERSITY DEPARTMENTS)
B.E. (Full Time) - END SEMESTER EXAMINATIONS, NOV/DEC 2023
ELECTRONICS AND COMMUNICATION ENGINEERING
5th Semester

EC5077 - REAL TIME EMBEDDED SYSTEMS
(Regulation 2019)

Time: 3hrs Max.Marks: 100

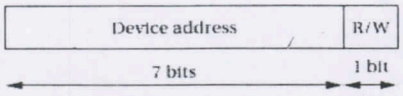
CO1	Ability to design and develop ARM processor based systems.
CO2	Ability to comprehend and appreciate the significance and role of microcontrollers in embedded systems.
CO3	Ability to analyze and demonstrate program design and optimization and proper scheduling of the process.
CO4	Ability to apply the concept of process, multi-processes and operating systems in embedded system design.
CO5	Ability to implement various communication protocols in distributed embedded computing platform.

BL – Bloom's Taxonomy Levels
(L1-Remembering, L2-Understanding, L3-Applying, L4-Analysing, L5-Evaluating, L6-Creating)

PART- A(10x2=20Marks)
(Answer all Questions)

Q.No	Questions	Marks	CO	BL
1	List out the characteristics of an embedded system.	2	CO1	L1
2	Write ARM assembly code to implement the C assignment: $y = (c - d) + (e - f)$.	2	CO1	L2
3	Mention the sources of CMOS power consumption.	2	CO2	L1
4	Calculate the average memory access time for a machine with a cache hit rate of 90% where the cache access time is 10 ns and the memory access time is 100 ns.	2	CO2	L2

5	For the basic block given below, rewrite it in single-assignment form, and also draw the data flow graph for that form.
	m = q – r;
	f = m + t;
	m = r + s;
	c = t – u;
		2	CO3	L2

6	Bring out the difference between clear box testing and black box testing.	2	CO3	L1
7	List out the functionalities that need to be performed by an operating system.	2	CO4	L1
8	Calculate the utilization over the hyper period of a set of processes given below Process / Period / Execution time P1 / $1.0 * 10^{-3}$ / $1.0 * 10^{-4}$ P2 / $1.0 * 10^{-3}$ / $2.0 * 10^{-4}$ P3 / $5.0 * 10^{-3}$ / $3.0 * 10^{-4}$	2	CO4	L2
9	What is the role of the session layer in ISO-OSI model?	2	CO5	L1
10	Compute the number of bits in the complete packet and time required to transmit the packet of I^2C bus runs at the rate of 1000 KB/s and that need to send one 8-bit byte. (Based on the message format shown in Figure 1.)  **Figure.1 Format of an I^2C address transmission.**	2	CO5	L2

PART- B(5x 13=65Marks)

Q.No	Questions	Marks	CO	BL
11.(a) (i)	With neat sketches, explain in detail about the structural and behavioral description of a toy train controller system.	7	CO1	L4
(ii)	Draw a state diagram for a behavior that sends the command bits on the track. The machine should generate the address, generate the correct message type, include the parameters, and generate the ECC.	6	CO1	L4
	OR			
11.(b)(i)	Draw the architecture of the ARM processor and explain briefly the functional blocks present in the ARM processor. Also, explain in detail about the various operating modes supported by the ARM processor	7	CO1	L4

(ii)	In the following code, show the contents of the ARM function call stack just after each C function has been entered and just after the function exits. Assume that the function call stack is empty when main() begins.
	int foo(int x1, int x2) {
	return x1 + x2;
	}
	int baz(int x1) {
	return x1 + 1;
	}
	int scum(int r) {
	for (i = 0; i = 2; i++)
	foo(r + i.5);
	}
	main() {
	scum(3);
	baz(2);
	m}
		6	CO1	L4

12.(a) (i)	Draw a timing diagram that shows a complete DMA operation, including handing off the bus to the DMA controller, performing the DMA transfer and returning bus control back to the CPU.	7	CO2	L3
(ii)	Discuss in detail about the various techniques that are used to overcome the switch bouncing problem in keyboard.	6	CO2	L3
	OR			
12.(b)	Discuss in detail about memory system mechanism and explain the basic types of cache organization with neat architecture diagram. Also briefly explain about the various types of cache misses and how it could be avoided?	13	CO2	L3
13.(a)(i)	Briefly explain the steps in the process of compilation.	7	CO3	L3

(ii)	Can you apply code motion to the following program?. Explain.
	for (i = 0; i < N; i++)
	for (j = 0; j < M; j++)
	z[i][j] = a[i] * b[i][j];
		6	CO3	L3

	OR			
13.(b)	With relevant examples, briefly explain about the various loop transformation techniques.	13	CO3	L3
14.(a)	Explain in detail about cooperative multitasking and preemptive multitasking.	13	CO4	L3
	OR			
14.(b)	With neat sketches, briefly explain about the various mechanisms used in Interprocess Communication.	13	CO4	L3

15.(a) (i)	With neat sketches and relevant examples, briefly perform an analysis on a system built for performing computation in a distributed embedded environment.	7	CO5	L4
(ii)	With taking suitable example, briefly explain about how single threaded mechanism and multithreaded mechanism are handled by the hardware accelerator.	6	CO5	L4
	OR			
15.(b)	With neat sketches, briefly explain how the bus that is used for automotive network handles data transaction and also discuss about the various error frames generated by nodes during data transmission.	13	CO5	L4

PART- C(1x 15=15Marks)

(Q.No.16 is compulsory)

Q.No	Questions	Marks	CO	BL
16.(i)	For the periodic processes shown below: Process | CPU time | Deadline P1 | 1 | 3 P2 | 1 | 4 P3 | 2 | 8 Schedule the processes using an EDF policy. Compute the schedule for an interval equal to the hyperperiod of the processes. Time starts at t=0.	9	CO4	L5
(ii)	With neat sketches and relevant examples, briefly explain about the predictive shutdown technique. Compare predictive shutdown technique with other techniques used by RTOS for power management.	6	CO4	L5