

10/10/2024

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ANNA UNIVERSITY (UNIVERSITY DEPARTMENTS)

B.E. /B.Tech / B. Arch (Full Time) - END SEMESTER EXAMINATIONS, NOV / DEC 2024



COMPUTER SCIENCE AND ENGINEERING
III Semester
CS23303 DIGITAL SYSTEM DESIGN

(Regulation 2023)

Time:3hrs

Max.Marks: 100

CO1	Use theorems and K-maps to simplify Boolean functions.
CO2	Design, analyze and implement combinational circuits.
CO3	Design, analyze and implement sequential circuits.
CO4	Design digital circuits using MSI chips and PLDs.
CO5	Use HDL to build digital systems.

BL – Bloom's Taxonomy Levels

(L1-Remembering, L2-Understanding, L3-Applying, L4-Analysing, L5-Evaluating, L6-Creating)

PART- A(10x2=20 Marks)

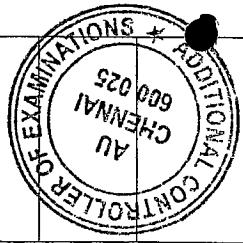
(Answer all Questions)

Q.No.	Questions	Marks	CO	BL
1	What are self-complementing codes? Give example.	2	1	2
2	Simplify the following Boolean expressions to a minimum number of literals (a) $ABC + A'B + ABC'$ (b) $(x + y)'(x' + y')$	2	1	3
3	Implement $pqr+qr'+p'q$ using NOR only.	2	2	3
4	Implement Full adder using MUX.	2	2	3
5	Show that a Johnson counter with n flip-flops produces a sequence of 2^n states. List the 10 states produced with five flip-flops and the Boolean terms of each of the 10 AND gate outputs.	2	3	4
6	How many flip-flop will be complemented in a 10-bit binary ripple counter to reach the next count after the count 1001100111?	2	3	4
7	Check whether the asynchronous sequential circuit for $Y = x_1x_2 + x_2y'$ is stable?	2	4	5
8	State the closed covering condition.	2	4	2
9	Obtain the 15-bit Hamming code word for the 11-bit data word 11001001010.	2	5	3
10	How many 32K * 8 RAM chips are needed to provide a memory capacity of 256K bytes?	2	5	4

PART- B(5x 13=65 Marks)

(Restrict to a maximum of 2 subdivisions)

Q.No.	Questions	Marks	CO	BL
11 (a)	i) Express the following numbers in decimal:	13	1	3



	(a) (10110.0101) ₂ (c) (DADA.B) ₁₆ ii) Simplify the following Boolean function F , together with the don't-care conditions d , and implement the simplified function using NAND gates only: (a) $F(x, y, z) = \sum(0, 1, 4, 5, 6)$ $d(x, y, z) = \sum(2, 3, 7)$	(b) (26.24) 8	
	OR		
11 (b)	Implement the following four Boolean expressions with three half adders: $D = A \oplus B \oplus C$ $E = A'BC + AB'C$ $F = ABC' + (A' + B')C$ $G = ABC$	13	1 3
12 (a)	A majority circuit is a combinational circuit whose output is equal to 1 if the input variables have more 1's than 0's. The output is 0 otherwise. (a) Design a 3-input majority circuit by finding the circuit's truth table, Boolean equation, and a logic diagram. (b) Write and verify a Verilog gate-level model of the circuit.	13	2 6
	OR		
12 (b)	Design a code converter that converts a decimal digit from BCD to 8, 4, -2, -1 code	13	2 6
13 (a)	A sequential circuit has two JK flip-flops A and B , two inputs x and y , and one output z . The flip-flop input equations and circuit output equation are $JA = Bx + B'y$ $KA = B'xy$ $JB = A'x$ $KB = A + xy$ $z = Ax'y + Bx'y$ (a) Draw the logic diagram of the circuit. (b) Tabulate the state table. (c) Derive the state equations for A and B .	13	3 5
	OR		
13 (b)	Using JK flip-flops, (a) Design a counter with the following repeated binary sequence: 0, 1, 2, 3, 4, 5, 6. (b) Draw the logic diagram of the counter.	13	3 5
14 (a)	An asynchronous sequential circuit has two internal states and one output given by, $Y_1 = x_1x_2' + x_1y_2' + x_2'y_1$ $Y_2 = x_2' + x_1y_1' + y_2 + x_1y_1$ & $z = x_2 + y_1$ Draw the logic diagram of the circuit. Obtain the flow table of the circuit.	13	4 3
	OR		
14 (b)	Explain with necessary illustration the techniques used for reduction of state and flow tables.	13	4 3
15 (a)	What is PLA? Tabulate the PLA programming table for the four Boolean functions listed below. Minimize the numbers of product terms and draw the design diagram. $A(x, y, z) = \sum(1, 3, 5, 6)$ $B(x, y, z) = \sum(0, 1, 6, 7)$ $C(x, y, z) = \sum(3, 5)$ $D(x, y, z) = \sum(1, 2, 4, 5, 7)$	13	5 3

(b)	<p>Define PAL. The following is a truth table of a three-input, four-output combinational circuit:</p> <table> <thead> <tr> <th>Inputs</th><th>Outputs</th></tr> <tr> <th><i>x y z</i></th><th><i>A B C D</i></th></tr> </thead> <tbody> <tr><td>0 0 0</td><td>0 1 0 0</td></tr> <tr><td>0 0 1</td><td>1 1 1 1</td></tr> <tr><td>0 1 0</td><td>1 0 1 1</td></tr> <tr><td>0 1 1</td><td>0 1 0 1</td></tr> <tr><td>1 0 0</td><td>1 1 1 0</td></tr> <tr><td>1 0 1</td><td>0 0 0 1</td></tr> <tr><td>1 1 0</td><td>1 0 1 0</td></tr> <tr><td>1 1 1</td><td>0 1 1 1</td></tr> </tbody> </table> <p>Tabulate the PAL programming table for the circuit, and mark the fuse map in a PAL diagram</p>	Inputs	Outputs	<i>x y z</i>	<i>A B C D</i>	0 0 0	0 1 0 0	0 0 1	1 1 1 1	0 1 0	1 0 1 1	0 1 1	0 1 0 1	1 0 0	1 1 1 0	1 0 1	0 0 0 1	1 1 0	1 0 1 0	1 1 1	0 1 1 1	13	5	3
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PART- C(1x 15=15 Marks)

(Q.No.16 is compulsory)

Q.No.	Questions	Marks	CO	BL
16.	Simplify using Tabulation method $F(A, B, C, D) = \sum (0, 2, 4, 5, 6, 7, 8, 10, 13, 15)$	15	1	5

