B.E (FT) END SEMESTER EXAMINATIONS – APR/ MAY 2024

Computer Science and Engineering

Fourth Semester

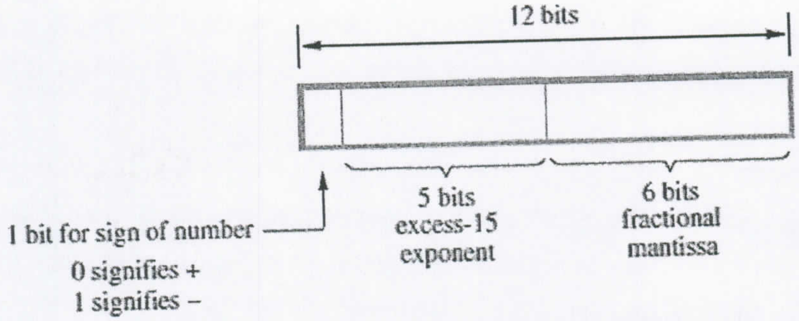
CS6107 – COMPUTER ARCHITECTURE

(Regulation 2018 - RUSA)

Time: 3 Hours	Answer ALL Questions	Max. Marks 100

Note: Assume data, if required

PART-A (10 x 2 = 20 Marks)

1.	Give the steps to translate a program in high level language to machine code.	2
2.	Justify the usage of the different types of operands.	2
3.	Identify the addressing mode of sw instruction and illustrate it for sw $t1,16($t2).	2
4.	Give the instruction format lw instruction and illustrate it for lw $s0,32($t0).	2
5.	Justify the need for Carry lookahead adder and carry save adder.	2
6.	Consider that floating-point numbers are represented in a 12-bit format as shown in Figure 6; an implied base of 2 and a 5-bit, excess-15 exponent, with the two end values of 0 and 31 used to signify exact 0 and infinity, respectively. The 6-bit mantissa is normalized as in the IEEE format, with an implied 1 to the left of the binary point. Represent the number −0.012 in this format.  12 bits 5 bits excess-15 exponent 6 bits fractional mantissa 1 bit for sign of number 0 signifies + 1 signifies –	2
7.	Give the drawbacks of single-cycle implementation.	2
8.	Distinguish between 1-bit predictor and 2-bit predictor.	2
9.	Give the significance of the various fields of a page table entry.	2
10.	Compare and contrast the three methods of communication between the processor and I/O.	2

PART – B (8 x 8 = 64 marks)
(Answer any 8 questions)

11.	i.State the CPU Performance equation. Enumerate the factors that affect CPU performance.	8

ii.Assume that for a program, compiler A results in a dynamic instruction count of 1.0E9 and has an execution time of 1.1 s, while compiler B results in a dynamic instruction count of 1.2E9 and an execution time of 1.5 s.

a. Find the average CPI for each program given that the processor has a clock cycle time of 1 ns.

b. Assume the compiled programs run on two different processors. If the execution times on the two processors are the same, how much faster is the clock of the processor running compiler A's code versus the clock of the processor running compiler B's code?

c. A new compiler is developed that uses only 6.0E8 instructions and has an average CPI of 1.1. What is the speedup of using this new compiler versus using compiler A or B on the original processor?

12. Suppose FP square root (FPSQR) is responsible for 20% of the execution time of a critical graphics benchmark. One proposal is to enhance the FPSQR hardware and speed up this operation by a factor of 10. The other alternative is just to try to make all FP instructions in the graphics processor run faster by a factor of 1.6; FP instructions are responsible for half of the execution time for the application. The design team believes that they can make all FP instructions run 1.6 times faster with the same effort as required for the fast square root. Compare these two design alternatives using Amdahl's law. 8

13. i.Translate the following C code to MIPS. Assume that the variables f, g, h, i, and j are assigned to registers $s0, $s1, $s2, $s3, and $s4, respectively. Assume that the base address of the arrays A and B are in registers $s6 and $s7, respectively. Assume that the elements of the arrays A and B are 4-byte words: 8 (4+4)

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B[8] = A[i] + A[j];
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ii.Translate the following MIPS code to C. Assume that the variables f, g, h, i, and j are assigned to registers $s0, $s1, $s2, $s3, and $s4, respectively. Assume that the base address of the arrays A and B are in registers $s6 and $s7, respectively.

```
addi $t0, $s6, 4
add $t1, $s6, $0
sw $t1, 0($t0)
lw $t0, 0($t0)
add $s0, $t1, $t0
```

14. Write a MIPS ALP to store a set of n integers in an array and compute the sum of the n integers using a procedure. 8

15. Explain floating point addition with the circuit diagram and flow chart. 8

16.	Explain Booth's algorithm. Simulate Booth's algorithm to compute 6*(-4).	8
17.	Draw the sequential circuit for integer division and simulate the non-restoring division algorithm for computing 6/3.	8
18.	Illustrate (Draw and explain) the datapath for beq instruction.	8
19.	Explain how pipeline stall is implemented with a neat architecture diagram.	8
20.	Assume the latencies for the floating-point functional units as follows: add is 2 clock cycles, multiply is 6 clock cycles, and divide is 12 clock cycles. Using the code segment below, show what the status tables look like when the SUB. D instruction has committed. L.D F6,32(R2) L.D F2,44(R3) MUL.D F0,F2,F4 SUB.D F8.F6.F2 DIV.D F10,F0,F6 ADD.D F6,F8,F2	8
21.	Write short notes on Virtual Machines.	8
22.	Appraise the Redundant array of independent disks. Explain the various levels of RAID.	8
	PART – C (2 x 8 = 16marks)	
23.	Investigate the code segment given below to identify the possible hazards. List the hazards identified with justification and provide solution. Also draw the multiple-clock cycle diagram. add r1,r2,r3 lw r4, 0(r1) sw r4,12(r1) lw r2, 4(r1) sub r5,r2,r4 and r6,r2,r4 or r7,r2,r4 beq r5,r6 label and r2,r3,r5 or r6,r1,r7 add r8,r1,r9 label: xor r10,r1,r11	8

24.	Formulate the organization of word-addressable i) a 32K 4-word direct mapped cache ii) a 32K 4-way set associative cache. Assume that the main memory is addressed using 32 bits.	8